DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the:

electromagnetic shielding structure formed at least partially in on ore more redistribution layers formed on an integrate circuit die (for example claim 1 line 3)

redistribution metal layer (for example claim 1 line 7)

redistribution dielectric layer (for example in claim 1 line 8)

dielectric layer of the integrated circuit (for example in claim 1 lines 9-10)

passivation layer (for example in claim 3 line 2)

integrated circuit pads (for example in claim 4 line 2)

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5, 7-34, 36-39, 41-46 and 48-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 11, 13, 29, 41, and 48 recite the limitation "an electromagnetic shielding structure formed at least partially in one or more redistribution layers." It is unclear how the shielding structure is formed in one or more redistribution layers. As depicted in Figure 5A, shielding structure, surrounds circuit element 525, where the redistribution layers are represented as element 528. It is unclear how elements 502, 508, and 554 of the shielding structure are "formed at least partially in one or more redistribution layers."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 6,037,649 to Liou.

Regarding claim 13, as far as the claim can be understood, Liou discloses an apparatus comprising:

an electromagnetic shielding structure (Figures 3A-3B, elements S1, S2 and S3 respective via interconnects 24 and 27; col 4 lines 48-53) formed at least partially in one or more redistribution layers (isolation layers such as 26 and 23 and metal layers such as S1,S1,S3, M1,M2, M3 provide for electrically redistribution of current) formed on an integrated circuit die (10), the electromagnetic shielding structure (elements S1, S2 and S3 respective via interconnects 24 and 27) substantially surrounding a circuit element (shielding substantially surrounds circuit element that is a inductor made in metal layers M1, M2, M3),

wherein the electromagnetic shielding structure has a top plate (S3, for example), a bottom plate (S2, for example), and sidewalls (vias 27, for example),

wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by via structures (27) on the integrated circuit die (10).

Regarding claim 14, as far as the claim can be understood, Liou discloses the apparatus of claim 13 wherein the sidewalls (vias 24, 27) of the electromagnetic shield structure (S1, S2, S3 and respective via interconnects) are formed at least in part by solid via structures (24, 27) in the redistribution layers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,037,649 to Liou in view of U.S. Pat. No. 6,847,282 to Gomez et al. (Gomez).

Regarding claim 11, as far as the claim can be understood, Liou discloses an apparatus comprising:

an electromagnetic shielding structure (Figures 3A-3B, elements S1, S2 and S3 respective via interconnects 24 and 27; col 4 lines 48-53) formed at least partially in one or more redistribution layers (isolation layers such as 26 and 23 and metal layers such as S1,S1,S3, M1,M2, M3 provide for electrically redistribution of current) formed on an integrated circuit die (10), the electromagnetic shielding structure (elements S1, S2 and S3 respective via interconnects 24 and 27) substantially surrounding a circuit element

(shielding substantially surrounds circuit element that is a inductor made in metal layers M1, M2, M3),

wherein the electromagnetic shielding structure has a top plate (S3, for example), a bottom plate (S2, for example), and sidewalls (vias 27, for example).

Liou fails to explicitly disclose the sidewalls of the electromagnetic shielding structure formed by under bump metal. Gomez discloses electromagnetic shielding structures formed by under bump metal (copper, col 3 lines 28-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Liou to have the electromagnetic shielding structure, including the sidewalls, be formed by under bump metal as in Gomez in order to provide for high conductivity in the shielding structure.

Regarding claim 12, Liou discloses the apparatus of claim 11 where the top plate (S3, for example) is support by via structures (vias 27, for example) formed in the redistribution layers (isolation layers such as 26 and 23 and metal layers such as S1,S1,S3, M1,M2, M3 provide for electrically redistribution of current).

Regarding claim 18, Liou discloses the apparatus of claim 11, where the redistribution layers include at least one redistribution metal layer (metal layers such as S1,S1,S3, M1,M2, M3) and at least one redistribution dielectric layer (isolation layers such as 26 and 23)

Response to Arguments

Applicant's arguments filed 03/07/2008 have been fully considered but they are not persuasive.

Objections to Drawings:

Applicant argues (pages 10-11) that the electromagnetic shielding structure formed by top plate 552, bottom plate 508, sidewalls 556 and 550 and rows of vias 564 and 562 illustrate the "*electromagnetic shielding structure formed at least partially in on ore more redistribution layers formed on an integrate circuit die"* (for example claim 1 line 3), "*formed above a passivation layer*" (for example in claim 3 line 2) "*formed above integrated circuit pads"* (for example in claim 4 line 2). Examiner notes that the Figure 5B does not include an integrated circuit die, integrated circuit pads or a passivation layer and thus do not show these features. The figure also does not label any portions of the shielding structure including redistribution layers. Redistribution layer 528 and 526 are depicted as being located within the circuit element 525 – it is unclear from the figures how the redistribution layers 528 and 526 contained within the circuit element apply to the shielding structure surrounding the element.

Applicant argues (pages 10-11) that the top plate 552, sidewalls 556 and 550 and regions between sidewalls 556 and 550 illustrate "redistribution metal layer (for example claim 1 line 7) "*the redistribution layers including at least one redistribution metal layer and at least one redistribution dielectric layer*" (for example in claim 1 line 7-8), However these drawing elements are not labeled to correspond to the claimed elements and the region between sidewalls 556 and 550 is not labeled at all.

Rejection under 35 USC 112:

Applicant argues (page 11-13) that the shielding structure formed at least partially in one or more redistribution layers is fully described in the specification. As depicted in Figures 5A/5B, shielding structure surrounds circuit element 525, where the redistribution layers are represented as element 526 and 528. It is unclear how elements 502, 508, and 554 of the shielding structure are "formed at least partially in one or more redistribution layers." The recited portions of the specification presented in applicants remarks discuss the top plate formed in a redistribution layer but the claim language is still unclear because the applicant's disclosure including the drawings does not depict redistribution layers in the shield structure.

Rejection under 35 USC 102 & 35 USC 103:

Applicant argues (page 13-18) that Liou teaches a structure formed in a conventional integrated circuit technology but the claims require the structure formed in redistribution layers. Applicant also includes specific references from the specification regarding the interpretation of "redistribution layer" to be defined as "used to route electrical connections between contact pads on an IC die and a location of a package contact" and having "thickness substantially greater than thicknesses of typical dielectric and conductive layers". Examiner acknowledges the interpretation of redistribution layers presented in the specification, but applicant has not lexicographically defined the redistribution layers to be limited to strict interpretation. The specification's discussion of redistribution layers does not limit the redistribution layers to being only above a

passivation only or only about an integrated circuit bonding pad or only having thicknesses greater than typical dielectric and conductive layers. *Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).* Thus these features described in the specification described for redistribution layers should not be imported into the claims. Furthermore the definition of "used to route electrical connections between contact pads on an IC die and a location of a package contact" does define the function of Liou's circuit layers and the thickness of the layers is not claimed. Examiner further notes that the term "redistribution layers" will be interpreted broadly in accordance with MPEP 2106, *USPTO personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)*.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811